

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Sridharan, et al.

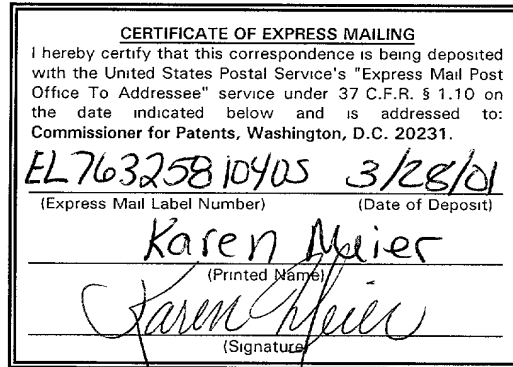
Title: METHOD OF AND APPARATUS  
FOR PERFORMING MODULATION

Appl. No.: unknown

Filing Date: Unknown

Examiner: Unknown

Art Unit: unknown



**AMENDMENT**

Commissioner for Patents  
Box PATENT APPLICATION  
Washington, D.C. 20231

Sir:

Please amend the application as follows:

**IN THE SPECIFICATION:**

On page 3, delete paragraph [0005], and replace this paragraph with the following in accordance with 37 C.F.R. §1.121. A marked up version showing changes is attached:

**[0005]** Certain conventional modulation schemes, such as quadrature modulation (QM), simultaneously modulate a carrier wave in accordance with two distinct bits of data or streams of information. Quadrature modulation digitally encodes multiple data streams independently. The two digitally encoded data streams are referred to as an in-phase (I) signal associated with I data and a quadrature (Q) phase signal associated with Q data. The I and Q data can be generated digitally. The combination of the I and Q signal results in a unique two-dimensional signal vector or symbol.

On page 6, delete paragraph [0023], and replace this paragraph with the following in accordance with 37 C.F.R. §1.121. A marked up version showing changes is attached:

**[0023]** Modulator 14 receives the data provided on inputs 16 and 18 and provides a modulated signal at output 21. The modulated signal can be a radio frequency (RF) signal for transmission over a wireless medium, such as, through an antenna 22. Alternatively, the modulated signal can be provided through a wire, a fiber optic cable or over other mediums.

On page 8, delete paragraph [0029], and replace this paragraph with the following in accordance with 37 C.F.R. §1.121. A marked up version showing changes is attached:

**[0029]** With reference to FIGURE 2, modulator 14 of communication system 10 includes a phase or frequency modulator circuit 20. Circuit 20 includes sigma delta ( $\Sigma\Delta$ ) control circuit 22, a phase lock loop (PLL) 24, and a voltage controlled oscillator (VCO) 26. Using a sigma delta control circuit such as circuit 22 provides advantages with respect to the precision and timing of the phase modulation. Sigma delta ( $\Sigma\Delta$ ) control circuit 22 can also be used to impart frequency modulation. Alternatively, circuit 20 can be replaced with any other circuits which provide precise phase/frequency modulation.

On page 9, delete paragraph [0035], and replace this paragraph with the following in accordance with 37 C.F.R. §1.121. A marked up version showing changes is attached:

**[0035]** Gain control or power amplifier 32 can be a power amplifier having a variable power supply voltage. Alternatively, amplifier 32 can be a variable gain amplifier having a control input that controls the gain of the amplifier. Preferably, the amplitude of the modulated wave signal at output 21 is directly proportional to the

amplitude data. The phase of the modulated signal at output 21 is preferably the same phase as the signal at input 34.

On page 11, delete paragraph [0041], and replace this paragraph with the following in accordance with 37 C.F.R. §1.121. A marked up version showing changes is attached:

**[0041]** With reference to FIGURE 6, modulator 14 is calibrated by providing data on inputs 16 and 18 so that the amplitude data is minimum at the same time the phase data represents a reversal as shown on modulated wave form or signal 304. Modulated waveform 304 is preferably a filtered binary phase shift keyed signal due to its simplicity for demodulation. Alternatively, any complex modulation waveform can be chosen where a precise timing relationship between phase and amplitude can be easily demodulated.

On page 14, delete paragraph [0055], and replace this paragraph with the following in accordance with 37 C.F.R. §1.121. A marked up version showing changes is attached:

**[0055]** A buffer 72 receives the amplitude data at input 18 and provides the buffered amplitude data to delay circuit 42. As discussed with reference to FIGURE 2, delay circuit 42 synchronizes the amplitude modulation by circuit 30 with the phase modulation of circuit 20 by delaying the amplitude data [as discussed above].

**IN THE CLAIMS:**

In accordance with 37 C.F.R. § 1.121, please substitute for original claims 3, 5, and 13, the following rewritten versions of the same claims, as amended. The changes are shown explicitly in the attached "Version with Markings to Show Changes Made".

1           3.     The method of claim 2, wherein the calibration scheme includes  
2     providing the modulated signal having a desired characteristic wherein the phase  
3     modulation is reversed when the amplitude modulation is minimum.

1           5.     The method of claim 4, wherein the calibration scheme includes  
2     detecting a delay between the phase modulation being reversed and the  
3     amplitude modulation being minimum.

1           13.    The method of claim 12, wherein the delay circuit is calibrated by  
2     providing the modulated signal having a desired characteristic, the desired  
3     characteristic being when the phase modulation is reversed and the amplitude  
4     modulation being simultaneously minimum; and detecting a delay between the  
5     phase modulation being reversed and the amplitude modulation being minimum.

#### REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested. The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date 3-28-01

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**Marked up replacement paragraphs:**

**[0005]** Certain conventional modulation schemes, such as quadrature [amplitude] modulation (QM) [(QAM)], simultaneously modulate a carrier wave in accordance with two distinct bits of data or streams of information. Quadrature modulation digitally encodes multiple data streams independently. The two digitally encoded data streams are referred to as an in-phase (I) signal associated with I data and a quadrature (Q) phase signal associated with Q data. The I and Q data can be generated digitally. The combination of the I and Q signal results in a unique two-dimensional signal vector or symbol.

**[0023]** Modulator 14 receives the data provided on inputs 16 and 18 and provides a modulated signal at output 21. The modulated signal can be a radio frequency (RF) signal for transmission over a wireless medium, such as, through an antenna [19] 22. Alternatively, the modulated signal can be provided through a wire, a fiber optic cable or over other mediums.

**[0029]** With reference to FIGURE 2, modulator 14 of communication system 10 includes a phase or frequency modulator circuit 20. Circuit 20 includes sigma delta ( $\Sigma\Delta$ ) control circuit 22, a phase lock loop (PLL) 24, and a voltage controlled oscillator (VCO) 26. Using a sigma delta control circuit such as circuit 22 provides advantages with respect to the precision and timing of the phase modulation. Sigma delta ( $\Sigma\Delta$ ) control circuit 22 can also be

used to [impact] impart frequency modulation. Alternatively, circuit 20 can be replaced with any other circuits which provide precise phase/frequency modulation.

[0035] Gain control or power amplifier 32 can be a power amplifier having a variable power supply voltage. Alternatively, amplifier 32 can be a variable gain amplifier having a control input that controls the gain of the amplifier. Preferably, the amplitude of the modulated wave signal at output 21 is directly proportional to the amplitude data. The phase of the modulated signal at output 21 is preferably the same phase as the signal at input 34. [Also, the frequency of the signal at output 21 is preferably the same as the frequency of signal at input 34.]

[0041] With reference to FIGURE 6, modulator 14 is calibrated by providing data on inputs 16 and 18 so that the amplitude data is minimum at the same time the phase data represents a reversal as shown on modulated wave form or signal 304. Modulated waveform 304 is preferably a filtered binary phase shift keyed signal due to its simplicity for demodulation. Alternatively, any complex modulation waveform can be chosen where a precise timing relationship between phase and amplitude can be easily [demonstrated] demodulated.

[0055] A buffer 72 receives the amplitude data at input 18 and provides the buffered amplitude data to delay circuit 42. As discussed with reference to FIGURE 2, delay circuit 42 synchronizes the amplitude modulation by circuit 30 with the phase modulation of circuit 20 by delaying the amplitude data [as discussed above].

**Marked up rewritten claims:**

3. The method of claim 2, wherein the calibration scheme includes providing the modulated signal having a desired characteristic wherein the phase modulation is reversed when the amplitude modulation is [zero] minimum.

5. The method of claim 4, wherein the calibration scheme includes detecting a delay between the phase modulation being reversed and the amplitude modulation being [zero] minimum.

13. The method of claim 12, wherein the delay circuit is calibrated by providing the modulated signal having a desired characteristic, the desired characteristic being when the phase modulation is reversed and the amplitude modulation being simultaneously [zero] minimum; and detecting a delay between the phase modulation being reversed and the amplitude modulation being [zero] minimum.